Logic gates and truth tables

Define digital logic states for the lab we will use the following definitions for VTL (Virginia Tech Logic)

True =" 1" = voltage between 6.95V and 9V

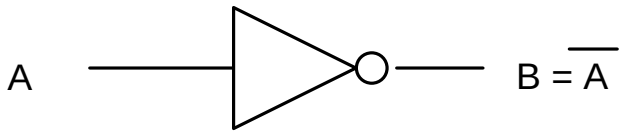
False = "0" = voltage between 0V and 2.95V

The **logic table** will show the possible input states (0 or 1) and the resultants output states.

Inverter (NOT function)

The circle denotes inversion or NOT. The bar over the logic variable denotes inversion.

$B = \overline{A}$ (NOT A) Inverted output.



Input A	Output B
0	1
1	0

Inverter logic table

Input A	Output B
False	True
True	False

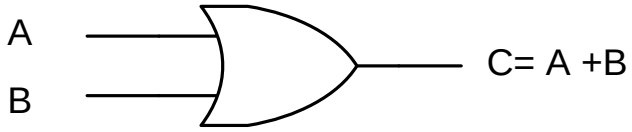
Inverter truth table

Input A	Output B
0V	9V
9V	0V

Inverter function table

OR function

C = A + B



Input A	Input B	Output C
0	0	0
0	1	1
1	0	1
1	1	1

OR gate logic table

Input A	Input B	Output C
False	False	False
False	True	True
True	False	True
True	True	True

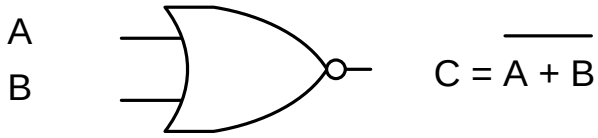
OR gate truth table

Input A	Input B	Output C
0V	0V	0V
0v	9V	9V
9V	0V	9V
9V	9V	9V

OR gate function Table

NOR function

$C = \overline{A + B}$ This is an OR function with resultant output inverted (not OR) NOR



Input A	Input B	Output C
0	0	1
0	1	0
1	0	0
1	1	0

NOR gate logic table

Input $\overline{A}$	Input $\overline{B}$	Output C
False	False	True
False	True	False
True	False	False
True	True	False

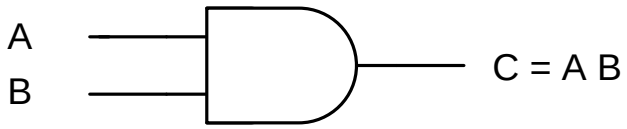
NOR gate truth table

Input A	Input B	Output C
0V	0V	9V
0V	9V	0V
9V	0V	0V
9V	9V	0V

NOR gate function table

AND function

C = A B



Input A	Input B	Output C
0	0	0
0	1	0
1	0	0
1	1	1

AND gate logic table

Input A	Input B	Output C
False	False	False
False	True	False
True	False	False
True	True	True

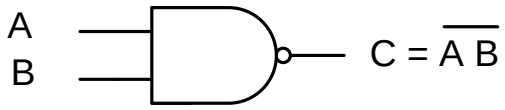
AND gate truth table

Input A	Input B	Output C
0V	0V	0V
0V	9V	0V
9V	0V	0V
9V	9V	9V

AND gate function table

NAND function

$C = \overline{A\,B}$ This is an AND function with resultant output inverted (not AND) NAND



Input A	Input B	Output C
0	0	1
0	1	0
1	0	0
1	1	0

NAND logic table

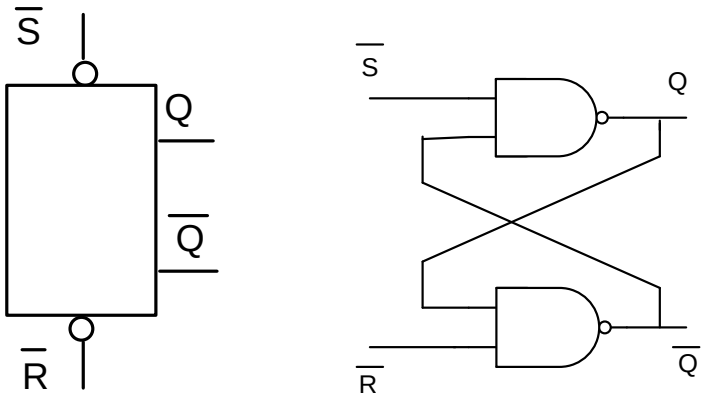
Input $\overline{A}$	Input $\overline{B}$	Output C
False	False	True
False	True	False
True	False	False
True	True	False

NAND truth table

Input A	Input B	Output C
0V	0V	9V
0V	9V	0V
9V	0V	0V
9V	9V	0V

NAND function table

S R Latch



The inputs set $\overline{S}$ and reset $\overline{R}$ will change the output Q and $\overline{Q}$ when they are taken low 0V. The outputs Q and $\overline{Q}$ are complementary of each other.

Note when both $\overline{S}$ and $\overline{R}$ inputs are at 0V when they are released back to 5V the output Q and $\overline{Q}$ will be determined by a race condition i.e. the last one to return to 5V will determine the output latch state

Input $\overline{S}$	Input $\overline{R}$	Output Q	Output $\overline{Q}$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	Q (No change)	$\overline{Q}$ (no change)

S R Latch Logic table

Input $\overline{S}$	Input $\overline{R}$	Output Q	Output $\overline{Q}$
0V	0V	9V	9V
0V	9V	9V	0V
9V	0V	0V	9V
9V	9V	Q (No change)	$\overline{Q}$ (no change)

S R Latch Function table