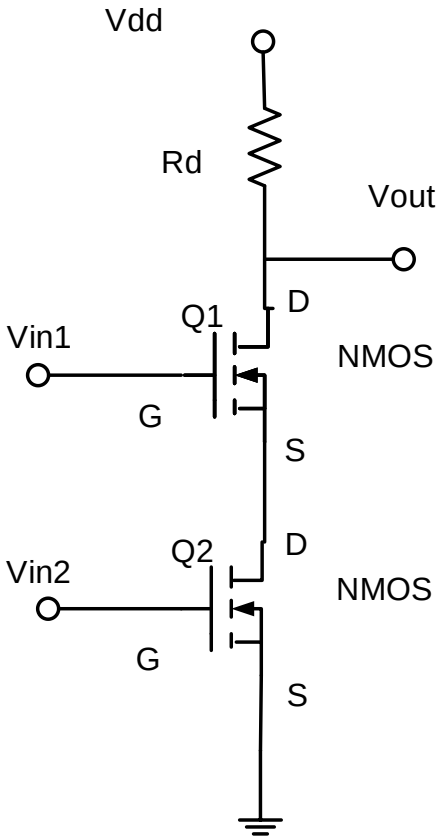
ECE2274
Pre-Lab for MOSFET logic LTspice
NAND Logic Gate, NOR Logic Gate, and CMOS Inverter
Include CRN # and schematics.

1. NMOS NAND Logic Gate

Use Vdd = 10Vdc. For the NMOS NAND LOGIC GATE shown below, use the 2N7000 MOSFET LTspice model that has a gate to source voltage Vgs threshold of 2V (Vto = 2.0). The input logic "1" = 10 volt and ground as a logic "0". Make a truth table showing the four possible combinations of Vin1 and Vin2 and the outputs. Choose Rd (drain current limit resistor) such that the drain currents of the NMOS devices will be about 30mA when the Vout is in a low state. Then run a DC .OP Bias Point simulation (use the added 2N7000 model in LTspice) on your design with the four possible input combinations for Vin1 and Vin2 to verify your gate. Observe the output voltage value for each input combination. Print your circuit schematic showing voltages for all four input combination.



NMOS NAND Logic Gate

2. NMOS NOR Logic Gate

Use Vdd = 10Vdc. Design an NMOS NOR logic gate using the 2N7000 MOSFET the model has Vto = 2.0 . Limit the drain current total to 30mA with a drain resistor (Rd). Show all work for your design and drawing. Then simulate your design in LTspice with DC .OP Bias Point simulations as you did for the NAND logic gate. Print out your circuit schematic showing voltages for all four input combination add from the view menu node voltage and drian current to display on the schematic. Also, fill in the truth table with all of the DC .OP Bias Point simulation voltage values.

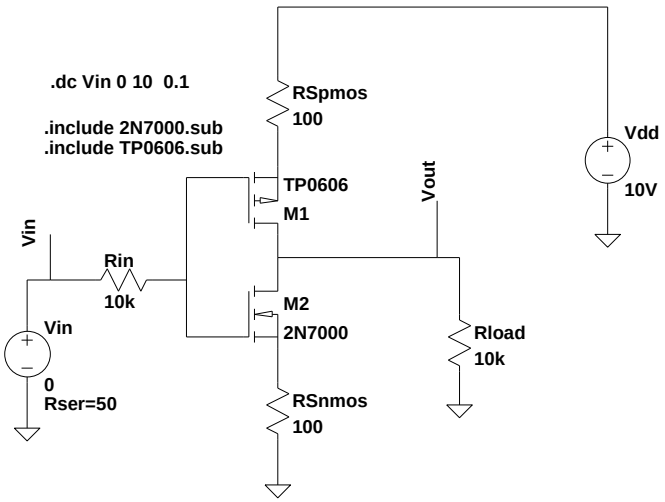
3. CMOS Inverter

Use VDD = 10Vdc. Design a CMOS inverter using a NMOS and PMOS FET. The drain current will be limited by the two external 100Ω source resistors (RSnmos, RSpmos). The MOSFETs that we use in the lab both have a V_{GS} threshold voltage of about $\left|2.0V\right|$ and internal resistance is RS = 0.2Ω. Assume that there is a input voltage level $2.0V < Vin < V_{DD} - 2.0V$ that will turn on both FETs at the same time. This will cause a large current flow that could damage the two devices. Because there is period of time when both devices on we will use a 1kHz triangle waveform as input so the time the devise send in a high current state will short in LTspice.

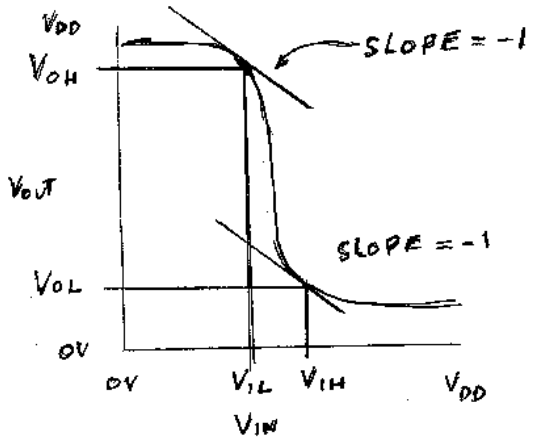
(Triangle Wave) Use LTspice to plot the input triangle waveform (PULSE) 0 to 10v, output voltage waveform, and the current thru the devices.

(DC sweep) Plot CMOS Transfer characteristic curve use DC sweep Vin from 0V to 10V. Plot Vout vs Vin mark on plot V_{OH} , V_{OL} , V_{IL} and V_{IH}.

V_{DD}	9Vdc
V_{in} (Triangle Wave) set PULSE	1kHz amplitude 0v to 10v Triangle wave PULSE 0V, 10V Tr=0.5ms Tf=0.5ms Tper=1ms, Td=0, Ton =1ns
V_{in} (DC Sweep)	0V to 10V 200mv step
Q1 PMOS	LTspice (TP0606) Lab (TP0606)
Q2 NMOS	LTspice (2N7000) Lab (2N7000)
LTspice TP0606 PMOS	Vto=-2 volts
Internal resistance	RS =0.2 ohms
LTspice 2N7000 NMOS	Vto = 2 volts
Internal resistance	RS = 0.2 ohms



CMOS inverter for LTspice



Cmos Transfer characteristic curve.

Required Attachments:
1. NAND Truth table.
2. Four schematics with voltages and currents of nodes and branches
3. NOR Truth table
4. Four schematics with voltages and currents of nodes and branches
5. Cmos Transfer characteristic curve (Triangle Wave), (DC sweep) 2 plots schematic.

Laboratory Exercise
MOSFET logic
NAND GATE, NOR GATE, and CMOS inverter

1. Build the NAND gate circuit from prelab on LTspice. Connect Vin1 and Vdd to 10V.

a. Run a DC Sweep of the NAND circuit by sweeping Vin2 from 0V to 10V with increments of 1V. Include the plot. Answer the question on the datasheet.

b. Change the voltage Vin2 to a pulse with Vinitial = 0V, Von = 10V, Trise = Tfall = 10u, Ton = 0.5m and Tperiod = 1m. This will produce a square wave from 0V to 10V. Run a transient simulation, plot the output voltage Vout from the NAND circuit, and answer the questions on the datasheet. Include the plot.

2. Build the NOR gate circuit from prelab on LTspice. Connect Vin1 and Vdd to 10V.

a. Run a DC Sweep of the NOR circuit by sweeping Vin2 from 0V to 9V with increments of 1V. Include the plot. Answer the question on the datasheet.

b. Change the voltage Vin2 to a pulse with Vinitial = 0V, Von = 10V, Trise = Tfall = 10u, Ton = 0.5m and Tperiod = 1m. Run a transient simulation and plot the output voltage Vout from the NOR circuit and answer the questions on the datasheet. Include the plot.

3. Build CMOS Inverter circuit on LTspice with both the external 100Ω source resistors to limit the current.

a. Run a DC sweep with the input from 0V to 10V in 200mv steps. Plot the Vout voltage and fill out the table in the datasheet. Include the plot.

b. Change the voltage Vin to a pulse with Vinitial = 0V, Von = 10V, Trise = Tfall = 10u, Ton = 0.5m and Tperiod = 1m. Run a transient simulation and plot the output voltage Vout from the Inverter circuit and answer the questions on the datasheet. Include the plot.

DATA SHEET MOSFET logic

Name: _____ CRN: _____

NAND GATE, NOR GATE, and COMS Inverter

1. NAND GATE

a. From the DC Sweep what is the input voltage at which the Vout starts to change?

b. i) What is the rise time? (time taken for the output to rise to 90% of the maximum value)

ii) What is the fall time? (time taken for the output to fall to 10% of the maximum value)

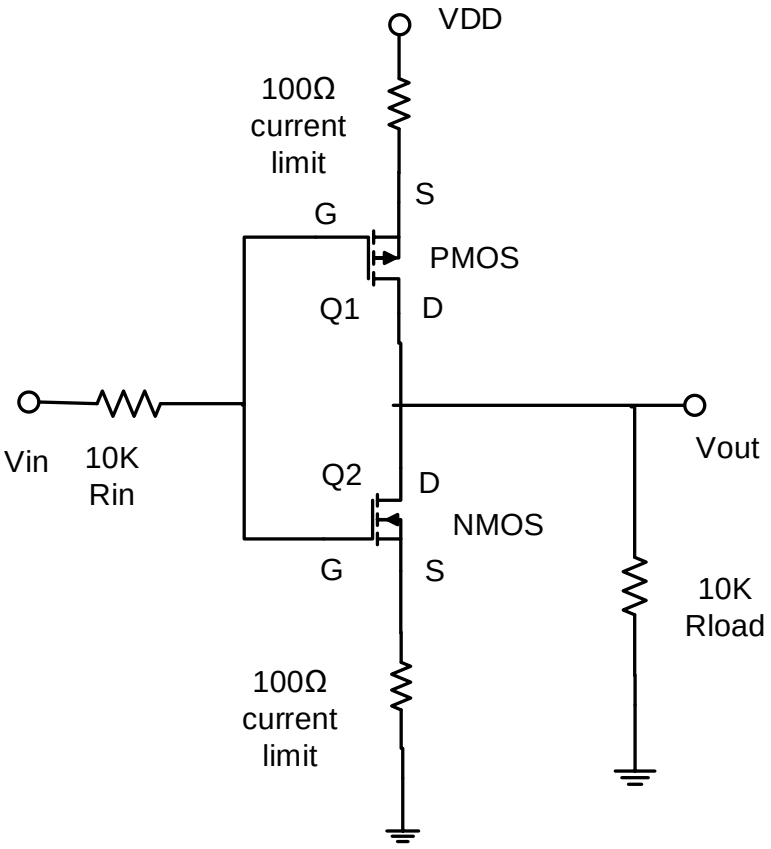
2. NOR GATE

a. From the DC Sweep what is the input voltage at which the Vout starts to change?

b. i) What is the rise time? (time taken for the output to rise to 90% of the maximum value)

ii) What is the fall time? (time taken for the output to fall to 10% of the maximum value)

3. CMOS Inverter



a. i) Table CMOS inverter static test. Vdd = 10Vdc

Vin	Vout
0v	
10v	

ii) Which device is on when the voltage is 0V?

iii) Which device is on when the voltage is 10V?

From DC sweep of CMOS inverter fill out the following table:

Name	Voltage
VOH	
VOL	
VIL	
VIH	

b. i) What is the rise time of the inverter?

ii) What is the fall time of the inverter?

Required Attachments:

1. DC Sweep of NAND gate
2. Transient Simulation of NAND Gate
3. DC Sweep of NOR Gate
4. Transient Simulation of NOR Gate
5. DC Sweep of Inverter
6. Transient Simulation of Inverter