Lecture on devices for ece2274 and charasistic curves

The LED used in the lab experiments has a forward voltage drop of about 1.8V. The student version of PSPICE does not have a LED in the library of parts. We will use a standard diode and a series 1.2Vdc voltage source to give us an equivalent LED diode. For the LED in LTspice use QTLP690C.

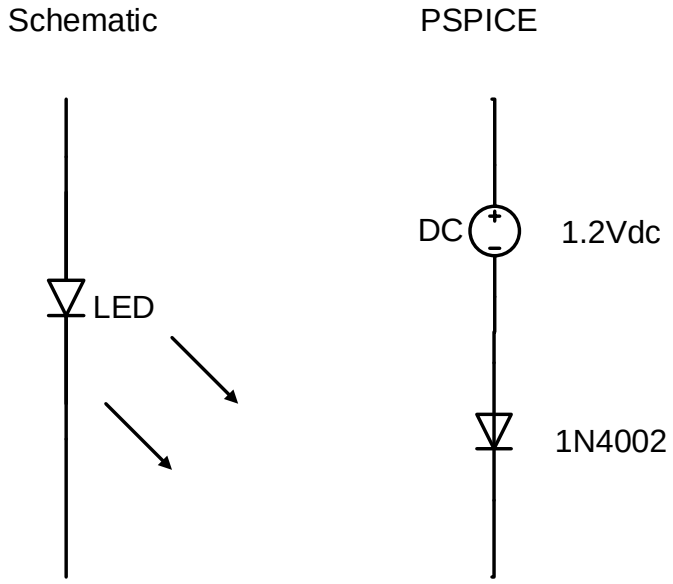


Figure 1

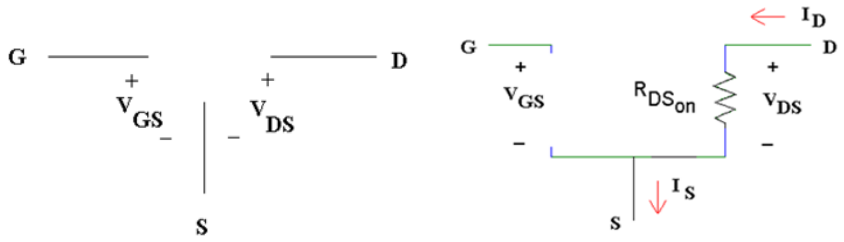
LED equivalent circuit for PSPICE designs

For our cmos discussions we will define a logic level of 0V to 9V with the low threshold of 2,0V and a high threshold of 7.0V. The logic family we will designate as VTL (Virginia Tech Logic).

Devices:

NMOS:

The NMOS FET that we use in the laboratory is a 2N7000 with the threshold voltage Vtn of 0.8V to 3.0V. For LTspice use 2N7000 which has the threshold voltage VTO = 2.0V The NMOS FET that we will use for PSPICE is IRF150 which has a threshold voltage VT0 = 2.8V We will edit the model so that the VTO = 2.0V for our designs in PSPICE.



Cut-Off
$V_{GS} < V_{TN}$

$I_D = I_S = 0$

Triode $I_G = 0$ $I_D < I_{Dsat}$
$V_{GS} > V_{TN}$ $V_{DS} < V_{GS} – V_{TN}$
$I_D = Kn[(V_{GS} – V_{TN})V_{DS} – 0.5V_{DS}^2]$
$R_{DSon} = V_{DS} / I_D$

Figure 2: NMOS enhancement mode models

In class assignment: print NMOS Curve and save for use in your designs

Generate the characteristic Curve for a NMOS (2N7000) in the non-saturated (Triode) region $V_{GS} > V_{TN}$, $V_{DS} < V_{DS}(sat)$, $V_{DS}(sat) = V_{GS} - V_{TN}$ and save for use in your designs. Draw on your curve a line thru the points $V_{DS}(sat) = V_{GS} - V_{TN}$ this will mark the separation of the (Triode) and (Saturated) regions. The designs of gates and switches are mainly operated in the cut off and non-saturated (Triode) region. The cut off region with Gate voltages below the threshold voltage (V_{TN}) will have a very low drain leakage current and drain to source voltage (V_{DS}) at the supply voltage. The non-saturated (Triode) region will have a gate to source voltage (V_{GS}) above the gate threshold voltage (V_{TN}) , V_{DS} below $V_{DS}(sat)$,and drain current (I_D) controlled the external circuit and V_{DS}.

Design for a drain current (I_D) that is larger than the current requirement based on the load that you need to drive (source or sink). The gate voltage (V_{GS}) must be selected such that your design is to the right of where the curves brake over to the horizontal part of the curve (the saturated region) in other words you want drive the gate voltage ($V_{GS} > V_{TN}$) high enough, such that the NMOS will be able to supply more current than you need for your load designs this will keep your NMOS in the triode region. The drain current is controlled be the external load (ie LED and resistor). From the curve you will be able to find the drain to source voltage (V_{DS}) at that load current (I_D).

Print from the curve tracer the characteristic for the NMOS 2N7000. Use Id max 20mA, offset 1.8V Vgs step 0.2V, and Vds max 0.5V Remember to use the cursor to mark one of the curves in middle of the graph to help you identify what is the value of that step.

You will have curve similar to the curve in figure 3.

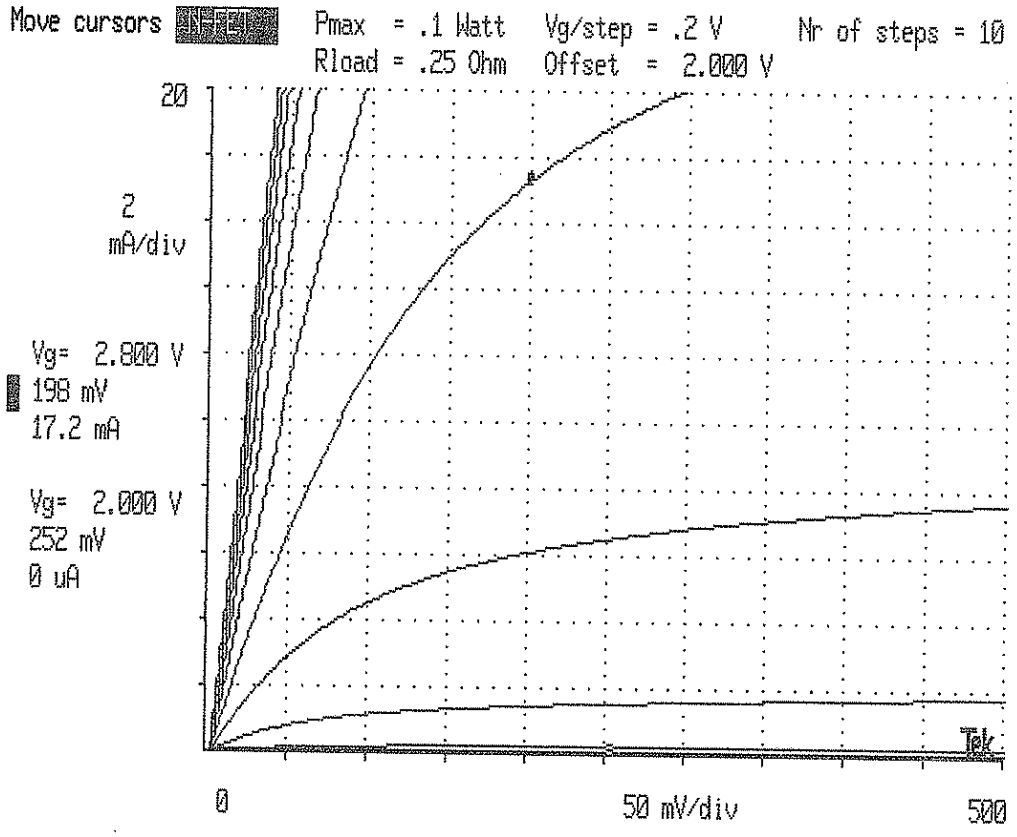
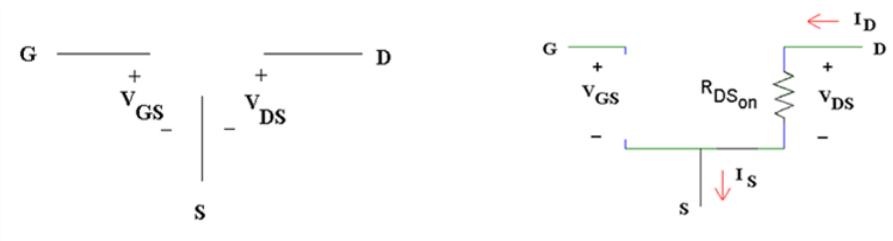


Figure 3: NMOS

PMOS:

The PMOS FET that we use in the laboratory is a TP0606 with the threshold voltage Vtn of -1.0V to -2.4V. The LTspice TP0606 has the VTO set to -2.1V. The PMOS FET that we will use for PSPICE is IRF9141 which has a threshold voltage VT0 = -3.2 V We will edit the model so that the VTO = -2.1V for our designs in LTspice.



Cut-Off	**Triode $I_G = 0$ $I_D < I_{Dsat}$**
$V_{GS} < V_{TP}$	**$V_{GS} < V_{TP}$ $V_{DS} > V_{GS} - V_{TP}$**
	$I_D = Kp[(V_{GS} - V_{TP})V_{DS} - 0.5V_{DS}^2]$
$I_D = I_S = 0$	**$R_{DSon} = V_{DS} / I_D$**

Figure 4:

PMOS enhancement mode models

In class assignment: print PMOS Curve and save for use in your designs

Generate the characteristic curve for a PMOS (TP0606) in the non-saturated (Triode) region $V_{GS} < V_{TP}$, $V_{DS} > V_{DS}(sat)$, $V_{DS}(sat) = V_{GS} - V_{TP}$ and save for use in your designs. Draw on your curve a line thru the points $V_{DS}(sat) = V_{GS} - V_{TP}$ this will mark the separation of the (Triode) and (Saturated) regions. The designs of gates and switches are mainly operated in the cut off and non-saturated (Triode) region. The cut off region will have a very low drain current mainly leakage and drain to source voltage (V_{DS}) at the supply voltage, with Gate voltages below the threshold voltage (V_{TP}). The non-saturated (Triode) region will have a gate to source voltage (V_{GS}) above the gate threshold voltage (V_{TP}) , V_{DS} below $V_{DS}(sat)$,and drain current (I_D) controlled the external circuit and V_{DS}.

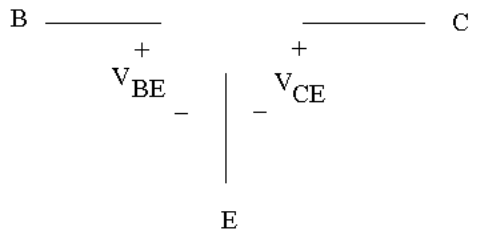
Design for a drain current (I_D) that is larger than the current requirement based on the load that you need to drive (source or sink). The gate voltage (V_{GS}) must be selected such that your design is to the right of where the curves brake over to the horizontal part of the curve (the saturated region) in other words you want drive the gate voltage ($V_{GS} < V_{TN}$) high enough, such that the PMOS will be able to supply more current than you need for your load designs this will keep your PMOS in the triode region. The drain current is controlled be the external load (i.e. LED and resistor). From the curve you will be able to find the drain to source voltage (V_{DS}) at that load current (I_D).

Print from the curve tracer the characteristic curve for the PMOS TP0606. Id max 20mA, offset 0V, Vgs step 1V, and Vds max 1v Remember to use the curser to mark one of the curves in middle of the graph help you identify what is the value of that step.

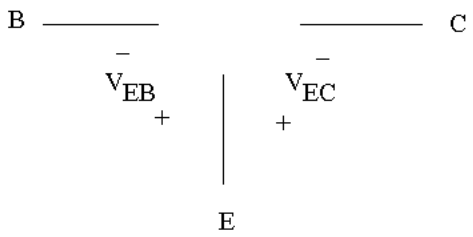
BJT:

The BJTs that we use in the lab are (NPN) 2N2222, 2N3904, and (PNP) 2N3906. These are available in your PSPICE.

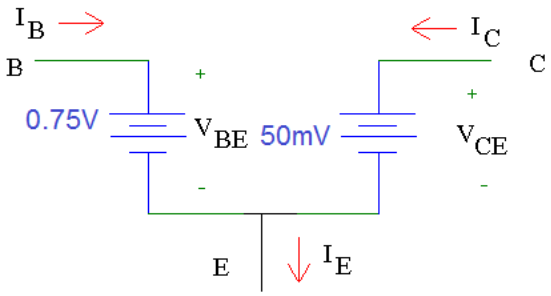
When designing BJTs (NPN, and PNP) for digital purposes the BJTs will either be cutoff or in the Saturated region. The cutoff region is where the input Ib =0 (base current) and the Vbe (base to emitter) voltage is below the base diode turn on voltage of about 0.7V. The saturated region is where the BJT is turned on hard enough to have the $I_C < \beta I_B$ and V_{CE} = 50 mV to 200mV at high currents. The collector current is set by the external resistance of the circuit.



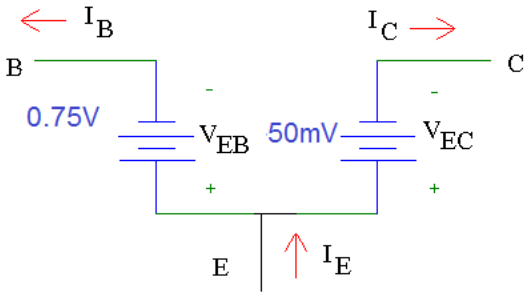
NPN Cut-Off



PNP Cut-Off



NPN Saturation



PNP Saturation

Figure 5

In class assignment: print BJT NPN Curve and save for use in your designs

Generate the Characteristic Curve for a BJT (2N2222) in the saturated region and save for use in your designs. The designs of gates and switches are mainly operated in the cut off and saturated regions. The cut off region will have a very low collector current, mainly leakage with Base voltage below the threshold voltage of 0.5V and with a base current = 0. The saturated region will have a base emitter voltage of the base emitter diode forward drop and a base current (I_B) above zero.

You need pick a collector current (I_C) for your designs based on the load that you need to drive. The base current (I_B) must be selected such that your design is to right of where the curves brake over to the horizontal part of the curve (the active region) in other words you want drive the base current (I_B) hard enough, such that the BJT will be able to supply more current than you need for your design this will keep your BJT in the saturated region. The collector current can now be controlled by the external load (LED and resistor).

From the curve you will be able to find the saturated collector to emitter voltage (V_{CE}) at that current (I_C).

Print from the curve tracer the characteristic for the BJT (NPN) 2N2222. Id max 20mA, Ib step 20uA and Vds max 500mv. Remember to use the curser to mark one of the curves in middle of the graph help you identify what is the value of that step.

You will have curve similar to the curve in figure 6

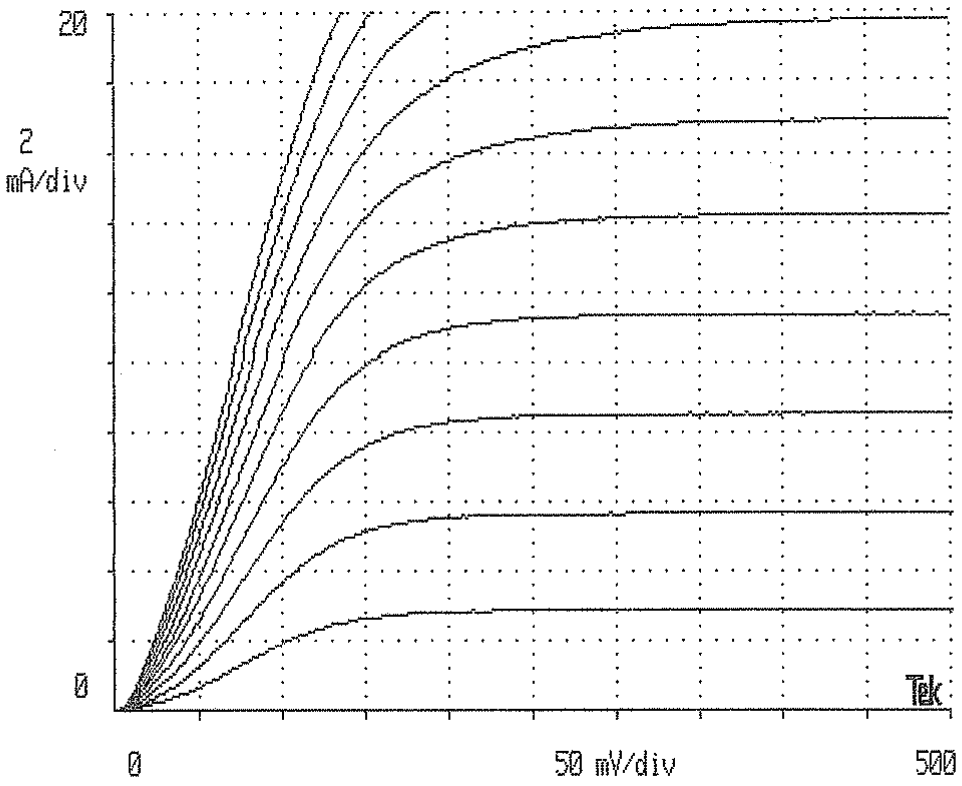


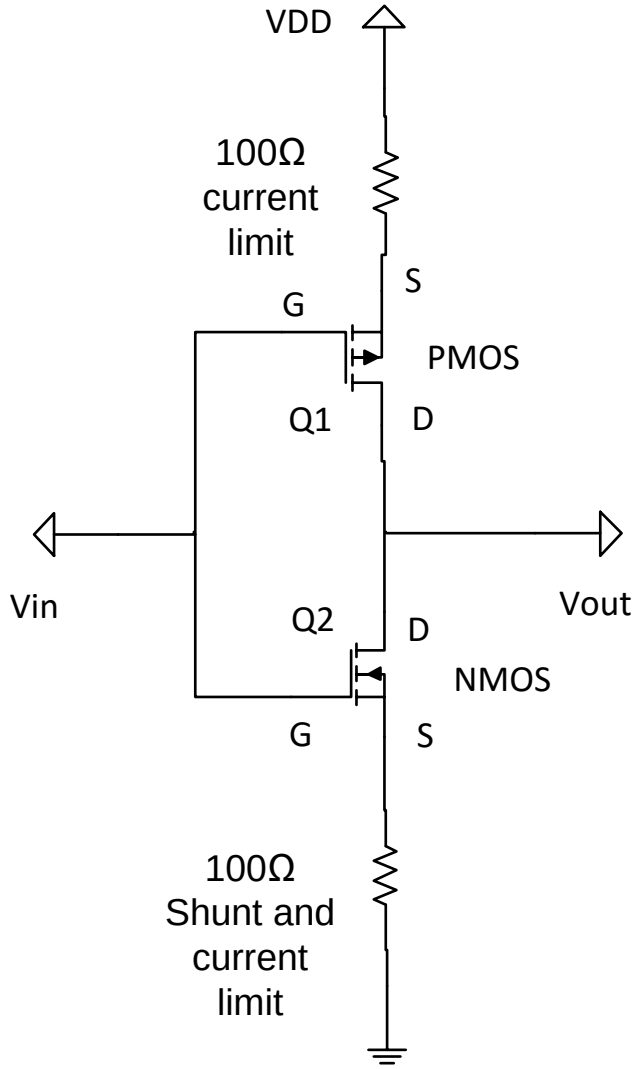
Figure 6: BJT

When designing with the enhance mode MOSFETs (NMOS, and PMOS) for digital purposes the MOSFETs will either be cutoff or in the triode region. The cutoff region is where the input Vgs (Gate to Source) voltage is below the threshold voltage (V_{TN} for NMOS, V_{TP} for PMOS). The triode region is where the MOSFET is turned on hard enough to have the $I_D < I_{Dsat}$ therefore the drain to source is a resistance of $R_D = V_{DS} / I_D$

CMOS inverter.

The NMOS and PMOS devices that we have in lab are power devices they have a low on series resistance. If we were to build the circuit below without the 100Ω resistors it would overheat because of high current flow in the transition region between the high and low state. The MOSFETs in a normal CMOS inverter would have an internal resistance high enough to pervert damage from overheating.

The CMOS circuit below has two external series resistors added in both source connections to limit the current and keep the results symmetrical. The lower 100Ω resistor will be used as shunt to monitor the current flow with a scale factor of 10ma/1v.



Logic gates and truth tables:

True =" 1" = voltage between 6.6v and 9V

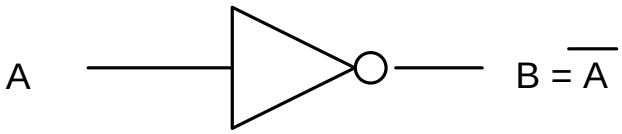
False = "0" = voltage between 0V and 2.8V

The **logic table** will show the possible input states (0 or 1) and the resultants output states.

Inverter (NOT function)

The circle denotes inversion or NOT. The bar over the logic variable denotes inversion.

$B = \overline{A}$ (NOT A) Inverted output.



Input A	Output B
0	1
1	0

Inverter logic table

Input A	Output B
False	True
True	False

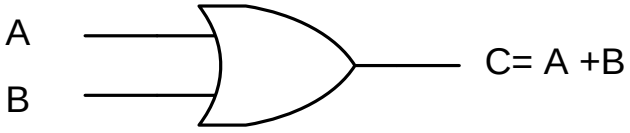
Inverter truth table

Input A	Output B
0V	9V
9V	0V

Inverter function table

OR function

C = A + B



Input A	Input B	Output C
0	0	0
0	1	1
1	0	1
1	1	1

OR gate logic table

Input A	Input B	Output C
False	False	False
False	True	True
True	False	True
True	True	True

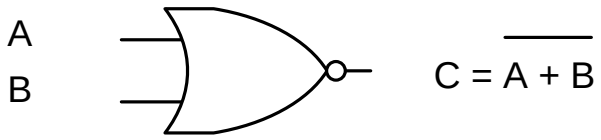
OR gate truth table

Input A	Input B	Output C
0V	0V	0V
0v	9V	9V
9V	0V	9V
9V	9V	9V

OR gate function Table

NOR function

$C = \overline{A + B}$ This is an OR function with resultant output inverted (not OR) NOR



Input A	Input B	Output C
0	0	1
0	1	0
1	0	0
1	1	0

NOR gate logic table

Input $\overline{A}$	Input $\overline{B}$	Output C
False	False	True
False	True	False
True	False	False
True	True	False

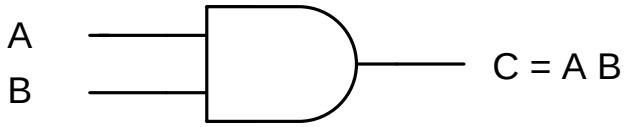
NOR gate truth table

Input A	Input B	Output C
0V	0V	9V
0V	9V	0V
9V	0V	0V
9V	9V	0V

NOR gate function table

AND function

C = A B



Input A	Input B	Output C
0	0	0
0	1	0
1	0	0
1	1	1

AND gate logic table

Input A	Input B	Output C
False	False	False
False	True	False
True	False	False
True	True	True

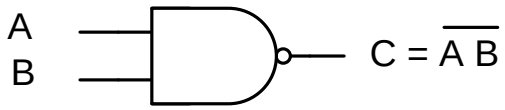
AND gate truth table

Input A	Input B	Output C
0V	0V	0V
0V	9V	0V
9V	0V	0V
9V	9V	9V

AND gate function table

NAND function

$C = \overline{A\,B}$ This is an AND function with resultant output inverted (not AND) NAND



Input A	Input B	Output C
0	0	1
0	1	1
1	0	1
1	1	0

NAND logic table

Input $\overline{A}$	Input $\overline{B}$	Output C
False	False	True
False	True	True
True	False	True
True	True	False

NAND truth table

Input A	Input B	Output C
0V	0V	9V
0V	9V	9V
9V	0V	9V
9V	9V	0V

NAND function table