Digital Logic Gates

Objective: This project will investigate the operation of BJT and MOSFET based digital logic gates.

Components: 2N2222 BJT (5), 2N7000 MOSFET (4), and 1N4001 diode

Introduction:

Two types of transistors commonly used in implementing logic circuits are BJTs and MOSFETs. In logic circuits, the transistor acts as a switch with two states – on and off. There are many characteristics used to evaluate the performance of logic circuits. Some of these characteristics are: power consumption, switching speed, noise margins, and fan-out. Noise margin is the maximum noise voltage that may be present in a gate without upsetting the proper operation of the circuit, i.e. maintaining correct logic levels 1 and 0. Fan-out specifies the number of standard loads that the output of a gate can drive and still maintain proper operation. One advantage of MOSFET logic gates is their high input impedance, and therefore low power consumption. BJT based gates (TTL) however have a faster switching time.

Figure 4-1 shows a two input TTL NAND gate. When used as an inverter, this NAND gates will have a transfer characteristic as shown in Figure 2. The low level and high level input and output values are indicated.

The output impedance of a fate is normally modeled by a combination of resistance and capacitance. This load model is applicable to any load including similar logic gates connected to the output. When the gate output switches from the low to the high state, the load capacitance must charge thus creating a propagation delay. The TTL NAND gate of Figure 3 is the same as the TTL and NAND gate of Figure 1 with a totem –pole output stage. The totem-pole output stage consists of a CC (with an additional 120 ohm resistor) stage stacked on top of a CE stage with a diode in between. The CE stage has the ability to sink large load currents and rapidly discharge the load capacitance. The CC sage with its low output impedance can source large load currents and quickly charge the load capacitance. Therefore higher speed operation and better drive capabilities are obtained thorough the totem pole output stage.

Figure 4 and 5 show a MOSFET NAND gate and NOR gate respectively. Notice that both these gates are implemented entirely through the use of MOSFETs without any resistors or diodes. The gate and drain of Q_1 in each circuit are connected together to imitate a biasing resistor. In this configuration, Q_1 acts as an active load for the circuit.

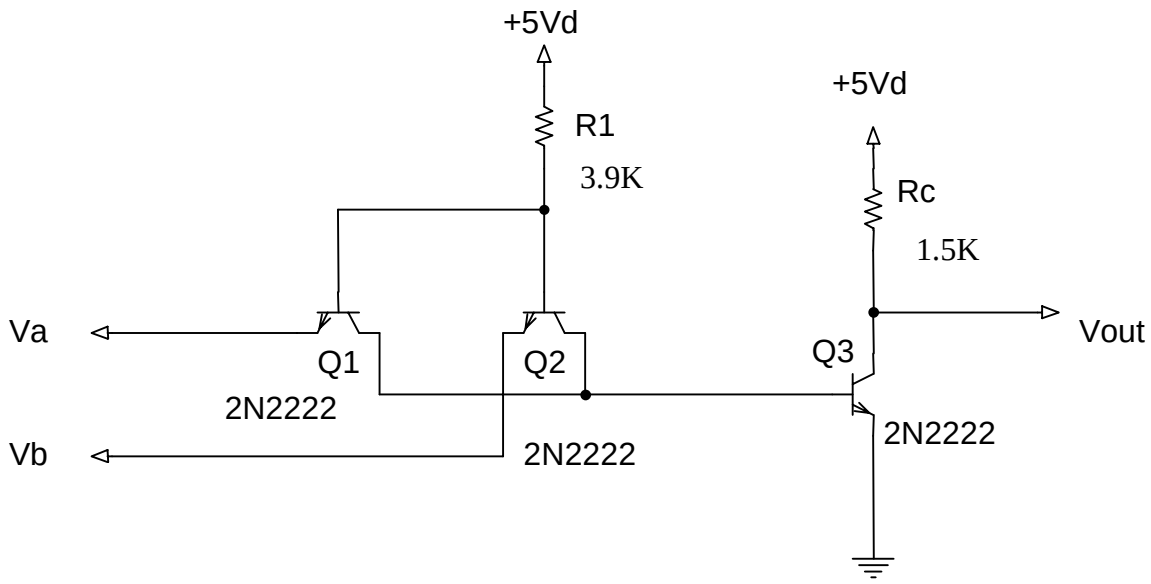

Figure 1: TTL NAND Gate

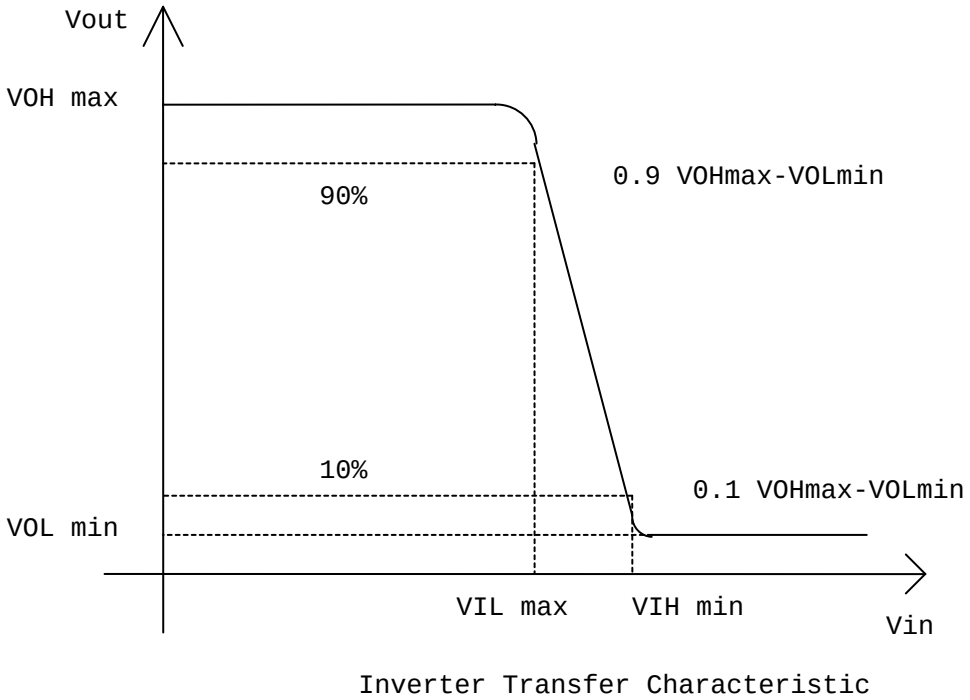

Figure 2: Inverter Transfer Characteristic

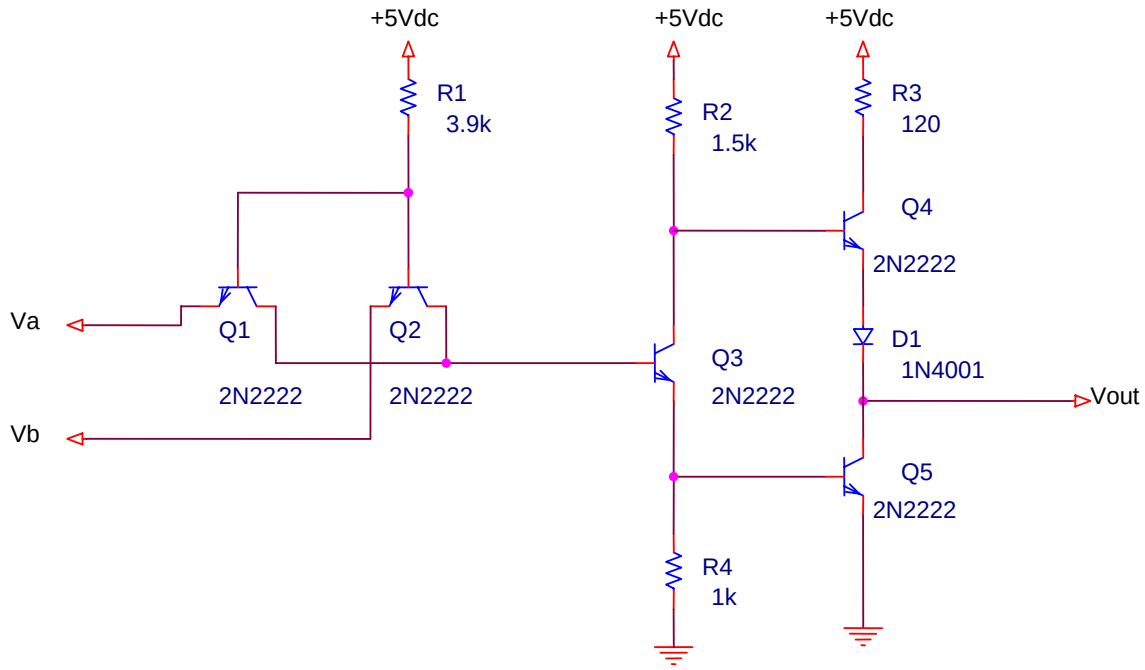

Figure 4 – 3: TTL NAND Gate with TOTEM POLE Output

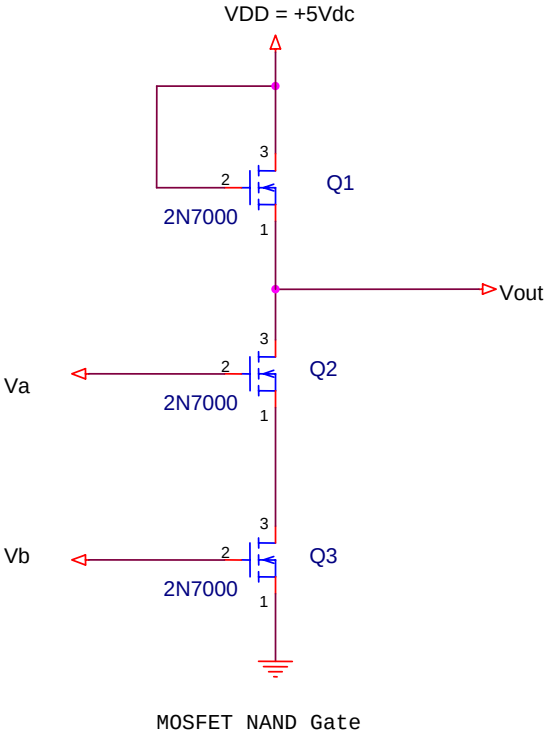

Figure 4: MOSFET NAND Gate

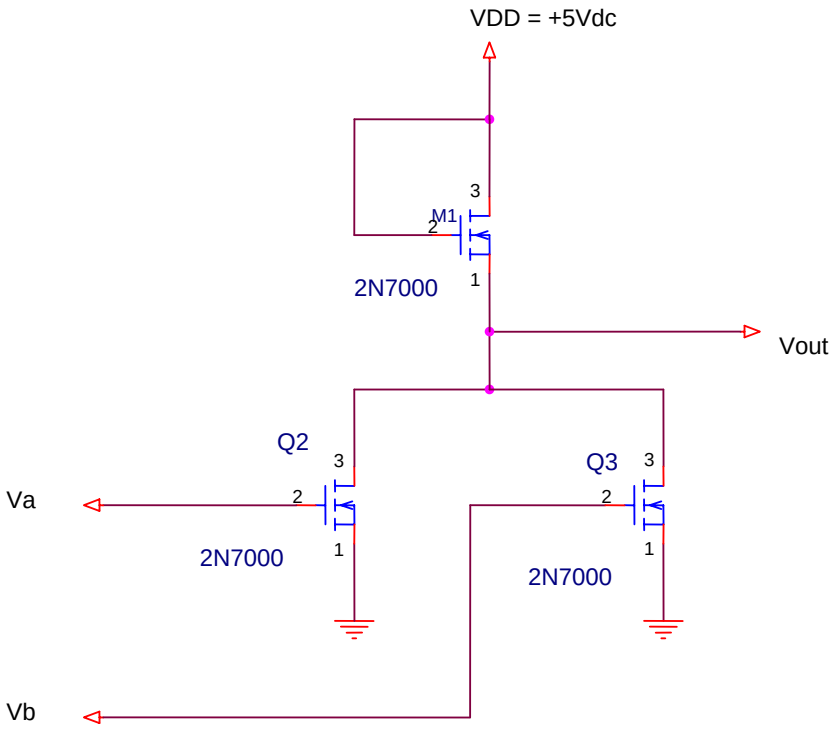

Figure 5: MOSFET NOR Gate

Design and Pre-Lab:

1. Verify the transfer characteristic of the TLL NAND, MOSFET NAND, and MOSFET NOR gates with PSPICE® use DC sweep analysis to sweep the input voltage with the inputs tied together. Sweep input from 0 to 5V and 5V to 0. Mark the inverter transfer characteristic on the plot: the 90% and 10% values. Use IRF150 for the MOSFET, Q2N2222 for the BJT and D1N4002 for the diode.

2. What are the functions of the diode and 120 Ω resistor serve in the TTL totem-pole output stage?

3. What is the primary reason MOSFET logic is slower than BJT based logic?

4. Design a MOSFET based logic circuit to achieve the function:

$$D = \overline{A + B \bullet C}$$

The design should minimize the number of MOSFETs required.

Lab Procedure:

1. Construct the TTL NAND gate of Figure 1. Verify its operation by completing a voltage truth table for the gate. Use 5 V for a high input and 0 V (ground) for a low input. Observe the output of the gate with the voltmeter.

2. Tie inputs A and B together to form an inverter. Use computer control to vary the input voltage from 0 to 5 V (you can actually see the necessary voltages by sweeping between 0 V and 2 V) and record the output voltage. Plot the transfer characteristic (V_O vs. V_I). Compare your transfer curve with Figure 2 to find the points V_{IL}, V_{OL}, V_{OH}, and V_{IH}.

3. With inputs A and B still tied together obtain a high output state. Place the decade resistance box between the output and ground. **Note: Always connect the power decade resistance box with the resistance set at the maximum value. Set the highest decade switch position to one then set the lower positions to the value that you want to test. Then change the highest position to zero and make the measurement. To try another value reset the highest position to 1 and then change the lower settings.** Vary the resistance until the output falls to 2.0 V. Determine the maximum high output load current (I_{OH}) the **source current** the current flowing out of the gate.

4. With inputs A and B still tied together obtain a low output state. Place the **power decade resistance** box (read connection note in Lab Procedure 3) between the 5 V supply and the output. Vary the resistance **(use the technique above)** until the output rises to 800 mV. Determine the maximum low output load current (I_{OL}) the **sink current** the current flowing into the gate.

5. Add the TOTEM-POLE output stage to the NAND gate to form the circuit of Figure 4-3. Verify its operation by completing a voltage truth table for the gate. You should also produce a plot of V_O vs. V_I using the lab software.

6. Repeat Lab Procedures 3, 4 for the TOTEM-POLE NAND gate. Compare the results with the previous case.

Note:

The MOSFET can be easily damaged by static electricity, so careful handling is important.

7. Construct the MOSFET NAND gate of Figure 4. Verify its operation by completing a voltage truth table for the gate and produce a plot of V_O vs. V_I using the lab software.

8. Have your design for the $D = \overline{A + B \bullet C}$ function verified by the instructor. Construct the circuit and verity its operation by completing a voltage truth table for the gate.

Questions:

1. Which output stage of the TTL NAND gate or the TOTEM POLE TTL NAND output allowed the largest sink current? Which has the largest source current?

2. Which logic family, TTL or MOSFET, allows the easiest logic implementations in an integrated circuit? Why?

Report Project 4 Digital Logic Gates.

Name:_____ Date_____ Lab Bench #_____

Remember to include all of your prelab assignment.

1. **TTL NAND**

   Low output V_{OL}=_____ High output V_{OH}=_____

V_A	V_B	V_{OUT}

What logic function is show by this truth table? _____

2. V_{IH} min=_____ V_{OL}=_____

   V_{IL} max=_____ V_{OH}=_____

3. V_{OUT}=_____ R_{LOAD}=_____Source I_{OH}=_____

4. V_{OUT}=_____ R_{LOAD}=_____Sink I_{OL}=_____

5. **TTL NAND Totem Pole Output**

   Low output V_{OL}=_____ High output V_{OH}=_____

V_A	V_B	V_{OUT}

What logic function is show by this truth table? _____

5-2. V_{IH} min=_____ V_{OL}=_____

   V_{IL} max=_____ V_{OH}=_____

6-3. V_{OUT}=_____ R_{LOAD}=_____Source I_{OH}=_____

6-4. V_{OUT}=_____ R_{LOAD}=_____Sink I_{OL}=_____

7. **MOSFET NAND**

Low output V_{OL}=_____ High output V_{OH}=_____

V_A	V_B	V_{OUT}

What logic function is show by this truth table? _____

V_{IH} min=_____ V_{OL}=_____

V_{IL} max=_____ V_{OH}=_____

8. $D = \overline{A + B \bullet C}$

Low output V_{OL}=_____ High output V_{OH}=_____

V_A	V_B	V_C	V_D

What logic function is show by this truth table? _____

Answer the questions at the end of the lab procedure and turn in with the report.